(*Please write your Exam Roll No.*) *Exam Roll No ……*

Bharati Vidyapeeth's
Institute of Computer Applications and Management
A-4, Paschim Vihar, New Delhi-63

SECOND SEMESTER [MCA] Internal Examination, March 2019

Paper Code: MCA - 106	**Subject: Operating Systems**
Time: 2 Hours	**Maximum Marks: 45**

Note: Section A is compulsory. Do any one question from each Unit.

SECTION - A

1. Answer all the following questions briefly:- 1.5 × 10 = 15

   (a) Compare the merits and demerits of overlays.

   (b) Inspect sleeping barber problem? Suggest a solution.

   (c) Formulate wait() and signal() atomic operations in semaphores without busy waiting?

   (d) Determine the dominant performance metrics in real time systems.

   (e) Justify how Clustered system assures reliability.

   (f) Differentiate between dispatcher and scheduler.

   (g) Identify use of stub in dynamic linking.

   (h) Assess problem in indirect Inter-process Communication and suggest any one solution to it.

   (i) In context of page replacement algorithm, which algorithm is implemented by stack algorithm? Write the one which exhibits Belady's anomal and the one that shows second chance algorithm.

   (j) Define semaphores. How is it better than test and set command?

SECTION – B (UNIT – I)

2. (a) Consider the following page reference string: 7.5

   7, 2, 3, 4, 7, 5, 6, 2, 1, 4, 5, 7, 3, 3, 7, 6, 3, 2, 1, 2, 3, 6, 5, 6, 4, 8, 7, 4

   Assume there are five frames. Formulate number of page faults that will occur for the following replacement algorithms: i) LRU Replacement, ii) FIFO Replacement, and iii) Optimal Replacement.

   (b) Explain the protocols by which the deadlock can be prevented. 7.5

OR

   (a) Propose a solution of the readers-writers problem using semaphores. 5

   (b) Discuss segmentation and compare it with paging. 5

   (c) Consider a system with a system with 32 bit logical address and 16 bit physical addresses and 1k page size. Compute size of page table. 5

SECTION – C (UNIT – II)

3. (a)

Processes	Burst time	Arrival time	Priority
P1	10	0	4
P2	15	2	3
P3	17	5	1
P4	25	5	5
P5	20	10	2

7.5

i) Make up Gantt charts for SJF (preemptive), priority (non-premptive) and Round Robin (quantum 5).

ii) Estimate average waiting time for each scheduling.

iii) Estimate average turnaround time for each scheduling.

(b) Compile the role of compiler, loader and memory management hardware in the following address scheme: i) compile time binding, ii) load time binding, and iii) run-time binding. 7.5

OR

(a) Suppose each memory allocation takes 170ns, and machine uses TLB that provides a 75% hit ratio. Formulate effective access time using paging. 5

i) Neglect the time required by TLB lookup

ii) ii) Assume that TLB takes algorithm 20ns

(b) Design a resource allocation graph using four process and four resources such that: i) the graph has a cycle and processes are deadlocked, and ii) the graph has a cycle but processes are not deadlocked. 5

(c) Explain Thrashing and propose its possible solutions. 5